Listing of claims:

1-38 Canceled.

39. (Previously presented) A method of forming an integrated circuit with circuitry under a bond pad, the method comprising:

forming devices in and on a substrate;

forming a first metal layer;

forming a first layer of relatively thick insulating material overlaying the first metal layer, wherein the thickness of the first layer of relatively thick insulating material strengthens the integrated circuit;

forming a top metal layer overlaying the relatively thick insulating layer; and

forming a bond pad on a surface of the top metal layer;

patterning the first metal layer to form gaps; and

wherein the gaps take up no more than 10% of the total area of the first metal layer under the bond pad.

40. (Previously presented) The method of claim 39, wherein the first layer of relatively thick insulating material is a layer of oxide having a thickness of at least 1.5 μm thick.

41. (Previously Presented) The method of claim 39, further comprising;

forming at least one intermediate metal layer between the devices and the first metal layer.

42. (Previously presented) The method of claim 39, wherein forming the top metal layer, further comprises:

forming a sub-layer of relatively stiff material.

43. (Previously presented) The method of claim 42 wherein the relatively stiff material is made form a layer of nitride.

44. (Previously presented) The method of claim 39, wherein the gaps are formed to be oriented such that the impact on the current flow through the first metal layer is minimized.

45. (Previously presented) A method of forming an integrated circuit with circuitry under a bond pad, the method comprising:

forming devices in and on a substrate;

forming a first metal layer;

forming a first layer of relatively thick insulating material overlaying the first metal layer, wherein the thickness of the first layer of relatively thick insulating material strengthens the integrated circuit;

forming a top metal layer overlaying the relatively thick insulating layer;

forming a bond pad on a surface of the top metal layer.

patterning the first metal layer to form gaps; and

wherein the gaps are formed to extend in a direction of a current flow in the first metal layer.

46. (Previously presented) A method of forming an integrated circuit with circuitry under a bond pad, the method comprising:

forming devices in and on a substrate;

forming a first metal layer;

forming a first layer of relatively thick insulating material overlaying the first metal layer, wherein the thickness of the first layer of relatively thick insulating material strengthens the integrated circuit;

forming a top metal layer overlaying the relatively thick insulating layer;

forming a bond pad on a surface of the top metal layer

forming a sub-layer of relatively stiff material; and

wherein the relatively stiff material is TiN.

47. (Previously presented) The method of claim 46, further comprising;

forming at least one intermediate metal layer between the devices and the first metal layer.

48. (Previously presented) The method of claim 46 further comprising:

patterning the first metal layer to form gaps.

49. (Original) The method of claim 46, wherein the relatively stiff material is formed near the first layer of relatively thick insulating material.

50. (Previously Presented) A method of forming an integrated circuit, the method comprising;

forming device regions in a substrate;

depositing a first metal layer overlaying the device regions;

patterning the first metal layer to form gaps, wherein the gaps extend in a current flow direction;

forming an insulating layer overlaying the first metal layer and filling in the gaps, wherein the gaps strengthen the integrated circuit by providing pillars of harder insulating material;

depositing a top layer of metal overlaying the insulating layer; and

forming a bond pad on a surface of the top layer of metal.

51. (Previously presented) The method of claim 50, wherein the insulating layer is a layer of oxide that is at least 1.5 μm thick.

52. (Original) The method of claim 50, wherein the gaps in the first metal layer take up no more than 10% of the total area of the metal line under the bond pad.

53. (Original) The method of claim 50, wherein forming the top metal layer further comprises:

forming a sub-layer of relatively stiff material adjacent the insulating layer.

54. (Original) The method of claim 53, wherein the relatively stiff material is TiN.

55. (Original) The method of claim 53, wherein the relatively stiff material is TiW.

56. (Original) The method of claim 53, wherein the relatively stiff material is made from a sub-layer of nitride.

57. (Canceled)

58. (Previously presented) A method of forming an integrated circuit, the method comprising:

forming device regions in and on a substrate;

forming a first metal layer overlaying the device regions;

forming an insulating layer overlaying the first metal layer;

forming a top metal layer overlaying the insulating layer including a sub-layer of relatively stiff material near the insulating layer, wherein the insulating layer is positioned directly between the first metal layer and the top metal layer;

forming a bonding pad on a surface of the top metal layer, and

wherein the sub-layer of relatively stiff material is TiN.

59. (Previously presented) A method of forming an integrated circuit, the method comprising:

forming device regions in and on a substrate;

forming a first metal layer overlaying the device regions;

forming an insulating layer overlaying the first metal layer;

forming a top metal layer overlaying the insulating layer including a sub-layer of relatively stiff material near the insulating layer, wherein the insulating layer is positioned directly between the first metal layer and the top metal layer;

forming a bonding pad on a surface of the top metal layer; and

wherein the relatively stiff material is TiW.

60. (Previously presented) The method of claim 62, wherein the sub-layer of the relatively stiff material is formed from a layer of nitride.

61. (Previously presented) The method of claim 58, wherein the insulating layer is an oxide layer having thickness of not less than 1.5 μm.

62. (Previously presented) A method of forming an integrated circuit, the method comprising:

forming device regions in and on a substrate;

forming a first metal layer overlaying the device regions;

forming an insulating layer overlaying the first metal layer;

forming a top metal layer overlaying the insulating layer including a sub-layer of relatively stiff material near the insulating layer, wherein the insulating layer is positioned directly between the first metal layer and the top metal layer;

forming a bonding pad on a surface of the top metal layer; and

wherein forming the first metal layer further comprises:

patterning the first metal layer to form gaps, wherein the gaps take up no more than 10% of a total layer area of the first metal layer under the bond pads.

63. (Previously presented) The method of claim 62, further comprising:

forming at least one intermediate metal layer between the first metal layer and the device regions; and

patterning the at least one intermediate metal layer to form interconnects between the devices.

64 – 65 Canceled.

66. (Previously presented) The method of claim 39, wherein forming devices in and on a substrate includes forming at least one of the devices under the bond pad.

67. (Previously presented) The method of claim 50, wherein the bond pad is formed directly over at least one of the device regions.

68-84 Canceled.

85. (Previously Presented) A method of forming an integrated circuit, the method comprising:

forming devices on and in a substrate;

forming at least one intermediate conductive layer overlaying the substrate;

forming at least one layer of insulating material separating the at least one conductive layers from each other;

forming a top conductive layer, the top conductive layer including at least one sub-layer of material that is relatively more stiff than the remaining top conductive layer; and

forming at least one bonding pad on the top conductive surface, wherein the at least one sub-layer of material that is relatively stiff is adapted to prevent the cracking of the one of more intermediate conductive layers under the at least one bonding pad so that one or more intermediate conductive layers under the at least one bonding pad can be used for functional interconnections of selected ones of the devices.

86. (Previously presented) The method of claim 85, wherein the sub-layer that is relatively stiff is made from one from a group of materials comprising TiN, SiN and TiW.

87. (Previously Presented) The method of claim 85, further comprising:

forming one of the at least one layer of insulating material between the top conductive layer and an intermediate conductive layer closest the top conductive layer to be relatively thicker than the remaining at least one layer of insulation.

88. (Previously Presented) The method of claim 85, further comprising:

forming gaps an in one of the at least one intermediate conductive layer to form pillars of relatively stiff insulating material passing through the one of the at least one intermediate conductive layer.

89. (Previously Presented) The method of claim 88, wherein the one of the at least one intermediate conductive layer is the intermediate conductive layer closest the top conductive layer.

90. (Previously presented) A method of forming an integrated circuit, the method comprising:

forming device regions on and in a substrate;

forming a first metal layer overlaying the substrate;

forming a top metal layer overlaying the first metal layer;

forming at least one bonding pad on the top metal layer; and

forming a first layer of insulating material separating the top metal layer from the first metal layer, wherein the first layer of insulating material has a thickness selected to resist cracking.

91. (Previously presented) The method of claim 90, wherein the first layer of insulating material is formed to be at least 1.5μm thick.

92. (Previously Presented) The method of claim 90, further comprising:

forming at least one intermediate metal layer between the first metal layer and the substrate; and

forming at least one insulation layer to separate the at least one intermediate metal layers from each other.

93. (Previously Presented) The method of claim 90, further comprising;

forming a sub-layer of material between the top metal layer and the first layer of insulating material, the sub-layer of material being relatively more stiff than the remaining top metal layer such that stresses on the top metal layer that occur during the formation of the at least one bonding pad are distributed over a larger area of the first layer of insulating material to reduce the probability of cracking the first layer of insulating material.

94. (Previously presented) The method of claim 90, further comprising:

forming gaps in the first metal layer to form pillars of relatively stiff insulating material passing through the first metal layer.

95. (Previously Presented) A method of forming an integrated circuit, the method comprising:

forming devices in and on a substrate;

forming a top conductive layer overlaying the substrate;

forming at least one bonding pad on the top conductive layer;

forming at least one intermediate conductive layer between the top conductive layer and the substrate;

forming at least one layer of insulating material separating the at least one conductive layers from each other; and

forming gaps in one of the at least one intermediate conductive layers closest the top conductive layer, the gaps being adapted to prevent cracking of the at least one intermediate conductive layers under the at least one bond pad by forming pillars of relatively stiff insulation

material passing through the one of the at least one intermediate conductive layer closest the top conductive layer, wherein the at least one intermediate conductive layers are adapted for functional interconnections of select devices under the bond pad.

96. (Previously Presented) The method of claim 95, wherein the gaps in the one of the at least one intermediate conductive layer closest the top conductive layer are formed in the direction of the current flow to reduce the effect of the gaps on the current flow.

97. (Previously Presented) The method of claim 95, further comprising:

forming a sub-layer of material between the top conductive layer and one of the layer of insulating material separating the one of the at least one intermediate conductive layer closest the top conductive layer from the top conductive layer, the sub-layer of material being relatively more stiff than the remaining top conductive layer such that stresses on the top conductive layer that occur during the formation of the at least one bonding pad are distributed over a larger area of the at least one layer of insulating material to reduce the probability of cracking the at least one layer of insulating material.

98. (Previously Presented) The method of claim 95, further comprising:

forming one of the at least one layers of insulating material between the top conductive layer and an intermediate conductive layer closest the top conductive layer to be relatively thicker than the remaining at least one layers of insulation.

99. (Previously presented) The method of claim 45, further comprising;

forming at least one intermediate metal layer between the devices and the first metal layer.

100. (Previously presented) The method of claim 45, wherein forming the top metal layer, further comprises:

forming a sub-layer of relatively stiff material.

101. (Previously presented) The method of claim 45, wherein forming devices in and on a substrate includes forming at least one of the devices under the bond pad.

102. (Previously presented) The method of claim 46, wherein forming devices in and on a substrate includes forming at least one of the devices under the bond pad.